CLAIMS

What is claimed is:

1. A data processing system comprising:

a first processor with a first operational characteristics on a system planar;

interconnection means for later connecting a second, heterogenous processor on said system planar, wherein said interconnection means enables said first processor and said second, heterogenous processor to collectively operate as a symmetric multiprocessor (SMP) system.

2. The data processing system of Claim 1, further comprising a second, heterogenous processor connected to said system bus via said interconnect means, wherein said second, heterogenous processor is comprises more advanced physical and operational characteristics than said first processor.

3. The data processing system of Claim 2, wherein said interconnection means supports backward compatibility of said second, heterogenous processor with said first processor.

4. The data processing system of Claim 3, wherein said interconnect means is coupled to a system bus and comprises a plurality of interrupt pins for connecting additional processors to said system bus.

5. The data processing system of Claim 4, further comprising an enhanced system bus protocol that enables said backward compatibility.

6. The data processing system of Claim 2, wherein said operational characteristics includes frequency, and said second, heterogenous processor operates at a higher frequency than said first processor.

7. The data processing system of Claim 6, wherein said operational characteristics includes an instruction ordering mechanism, and said first processor and second processor utilizes a different one of a plurality of instruction ordering mechanism from among in-order processing, out-of-order processing, and robust out-of-order processing.

8. The data processing system of Claim 2, wherein said more advanced physical topology are from among higher number of cache levels, larger cache sizes, improved cache hierarchy, cache intervention, and larger number of on-chip processors.

9. The data processing system of Claim 1, further comprising a switch that provides direct point-to-point connection between said first processor and later added processors.

10. A method for upgrading processing capabilities of a data processing system comprising:

providing a plurality of interrupt pins from a system bus on a system planar to allow later addition of other processors;

enabling direct connection of a new, heterogenous processor to said system planar via said interrupt pins; and

providing support for full backward compatibility by said new, heterogenous processor when said new processor comprises more advanced operational characteristics to enable said data processing system to operate as a symmetric multiprocessor system.

11. The method of Claim 7, wherein said providing support includes implementing an enhanced system bus protocol to support said new, heterogenous processor.

12. A multiprocessor system comprising:

a plurality of heterogenous processors with different operational characteristics and physical topology connected on a system planar;

a system bus that supports system centric operations;

interrupt pins coupled to said system bus that provide connection for at least one of said plurality of heterogenous processors;

an enhanced system bus protocol that supports downward compatibility of newer processors that support advanced operational characteristics from among said plurality of processors to processors that do not support said advance operation characteristics.

13. The multiprocessor system of Claim 12, further comprising a switch that provides direct point-to-point connection between each of said plurality of processors and later added processors.

14. The multiprocessor system of Claim 12, wherein said plurality of processors includes heterogenous processor topologies including different cache sizes, cache states, number of cache levels, and number of processors on a single processor chip.